WHAT IS CLAIMED IS

1. A differential oscillator circuit including first and second branches each connected between a high supply potential and a low supply potential, said first branch including, arranged in series:

- a first transistor having a control terminal, a first current terminal placed on the side of said high supply potential and a second current terminal placed on the side of said low supply potential; and

- first bias means for imposing a determined current through the first and second current terminals of the first transistor,

said second branch including, arranged in series:

- a second transistor having a control terminal, a first current terminal placed on the side of said high supply potential and a second current terminal placed on the side of said low supply potential; and

- second bias means for imposing said determined current through the first and second current terminals of the second transistor,

said first and second transistors being connected in a differential configuration, the first current terminal of the first transistor, respectively of the second transistor, being connected to the control terminal of the second transistor, respectively of the first transistor,

wherein said differential oscillator circuit further includes:

- an electro-mechanical resonator connected via first and second terminals between the first current terminal of the first transistor and the first current terminal of the second transistor, said first and second terminals of the electro-mechanical resonator forming first and second output terminals of the differential oscillator circuit; and

- a capacitive element of determined capacitance value which is connected between the second current terminal of the first transistor and the second current terminal of the second transistor,

the capacitance value of said capacitive element being selected so as to be less than a maximum value above which relaxation of the oscillator circuit can occur.

2. The differential oscillator circuit according to claim 1, wherein said maximum value is defined as the value for which reactance of the oscillator circuit is null at a null frequency.

3. The differential oscillator circuit according to claim 1, wherein said capacitance value of the capacitive element is selected to be close to said maximum value, preferably between 80% and 100% of said maximum value.

4. The differential oscillator circuit according to claim 1, wherein a ratio between a capacitance value C_L seen between the first current terminals of said first and second transistors and a shunt capacitance C_O of said electro-mechanical resonator is minimized.

5. The differential oscillator circuit according to claim 4, wherein said capacitance value C_L seen between the first current terminals of said first and second transistors is reduced to parasitics.

6. The differential oscillator circuit according to claim 1, wherein said first bias means include a first current source connected between the second current terminal of said first transistor and said low supply potential and a first resistor means connected between the first current terminal of said first transistor and said high supply potential,

and wherein said second bias means include a second current source connected between the second current terminal of said second transistor and said low supply potential and a second resistor means connected between the first current terminal of said second transistor and said high supply potential.

7. The differential oscillator circuit according to claim 1, wherein said first bias means include a first current source connected between the first current terminal of said first transistor and said high supply potential and a third transistor comprising a control terminal and first and second current terminals which are respectively connected to the first terminal of said first transistor, the second terminal of said first transistor and said low supply potential,

and wherein said second bias means include a second current source connected between the first current terminal of said second transistor and said high supply potential and a fourth transistor comprising a control terminal and first and second current terminals which are respectively connected to the first terminal of said second transistor, the second terminal of said second transistor and said low supply potential.

8. The differential oscillator circuit according to claim 7, wherein said first and second current sources are respectively fifth and sixth transistors each comprising a control terminal and first and second current terminals and forming part of a current mirror,

the first current terminals of said fifth and sixth transistors being connected to said high supply potential,

the second current terminal of said fifth transistor, respectively of said sixth transistor, being connected to the first terminal of said first transistor, respectively of said second transistor.

9. The differential oscillator circuit according to claim 8, further including an amplitude regulation loop connected to the terminals of said electro-mechanical resonator to enslave the current delivered by the current mirror comprising said fifth and sixth transistors.

10. The differential oscillator circuit according to claim 9, wherein said amplitude regulation loop includes two resistor means connected in series between the terminals of the electro-mechanical resonator.

11. The differential oscillator circuit according to claim 10, wherein said two resistor means are native transistors having a threshold voltage close to zero and operating in the sub-threshold region.

12. The differential oscillator circuit according to claim 10, wherein a connection node between said two resistor means is coupled to means for regulating the current delivered by said current mirror.

13. The differential oscillator circuit of claim 1, wherein said oscillator circuit is realized in CMOS technology.

14. The differential oscillator circuit of claim 1, wherein said electro-mechanical resonator is a bulk acoustic wave resonator.